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(54) Integrated receiver

(57) An integrated receiver in which in order to permit ac-coupling between stages and to remove the effects of strong directly detected amplitude modulated interfering signals lying within the input band of the receiver, the input signal is frequency down converted using a local oscillator signal which provides an intermediate frequency (F_{if}) which lies above the frequency of the directly detected interferer (F_{AMP}). The outputs from the frequency down converters (14, 16, 18, 20) are ac coupled to filtering means the outputs of which are applied to an equaliser (52). The filtering means may comprise a polyphase filter (50), the frequency response of which is distorted by the ac coupling capacitors (54, 56). By applying the outputs of the filtering means to the equaliser (52) substantially all the distortion introduced by the ac coupling capacitors (54, 56) on the filter response is removed to provide an acceptable signal for detection and recovery of the modulating signal.

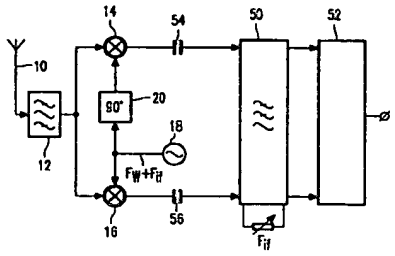

FIG. 6

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Description

The present invention relates to an integrated receiver having particular, but not exclusive, application in cellular and cordless telephony, paging and other applications requiring integrated receivers such as frequency analysers.

A typical architecture for an integrated receiver is a zero IF(ZIF) architecture in which a received signal is split into two paths and applied to respective mixers to which are applied a local oscillator signal having a frequency of such a value as to frequency down convert the received signal to a ZIF. A relative phase shirt of approximately 90° exists between the local oscillator signals applied to the respective mixers. The signal path from one of the mixers is designated an in-phase or I channel and that from the other of the mixers is designated as a quadrature or Q channel. The products of mixing in the I and Q channels are low pass filtered to derive the difference components which are thereafter demodulated.

A well known problem with ZIF receivers is that of dc offsets which occur due to the various stages being directly coupled and also due to some of the wanted products of mixing being at dc or close to it. The occurrence of dc offsets within the various stages leads to severe desensitizing the receiver circuit which inhibits direct coupling of these stages. Techniques for avoiding the effects of dc offsets include providing ac coupling circuits or more sophisticated dc blocking circuits between successive stages. Inevitably this can lead to loss of some of the wanted products of mixing. In the art, what is termed a notch is created in the frequency response on or about the ZIF. The width of the notch is typically a function of the capacitance value used in the ac coupling circuits. Thus to minimise the width of the notch, a high value capacitance is used. However the higher the value of capacitance the longer the ac-coupling time constant which in turn places a limit on the speed with which the receiver can recover from a change in dc offset caused by amplitude modulated or pulsed interfering signals. While the ac-coupling time constant can be reduced by using a lower value of capacitance, this causes the width of the notch to be greater thereby eliminating more of the wanted signals.

US Patent Specification 4,944,025 discloses a direct conversion FM receiver that includes ac-coupling and automatic gain control. The receiver receives a signal at a radio frequency, frequency down converts the received signal and filters the signal which is subsequently frequency up-converted and then demodulated. The frequency-down conversion, filtering and up-conversion is done using quadrature related mixers the respective outputs of which are successively ac-coupled to an amplifier, a low pass filter and a mixer. In order to overcome the problem of the notch in the frequency spectrum due to ac-coupling, the local oscillator frequency supplied in quadrature to the frequency down converting mixers is offset from the nominal carrier frequency of the received signal by the sum of the width of the notch plus the base bandwidth of the modulated signals. In a numerical example the offset corresponds to about a quarter of the channel spacing. The bandwidth of the low pass filters is such as to pass the band of the wanted signals but block signals on adjacent channels. Although the invention disclosed in US Patent Specification 4,944,025 goes some way to mitigating the problem due to the notch created by ac coupling, there are nevertheless constraints on the choice of value of the ac-coupling capacitors because if it is relaxed too far, inadequate image rejection occurs because as the offset frequency, which is a function of the size of the notch, increases the adjacent channel signals will be closer in frequency to the wanted signals and will be more difficult to separate by simple filtering.

Another problem which occurs with direct conversion receivers, and is not considered by US Patent Specification 4944025 is that of the presence of strong amplitude modulated signals in the rf signal bandwidth, which signals are directly detected and appear in the ZIF band and cannot be removed by filtering.

It is an object of the present invention to be able to relax the ac-coupling constraints in an integrated direct conversion receiver.

According to the present invention there is provided a receiver comprising means for frequency down-converting a received signal to produce quadrature related i.f. signals at a frequency offset from d.c, means for blocking dc-offsets in the quadrature related i.f. signals, means for recovering the wanted i.f. signals and means for equalising the wanted i.f. signals and detecting modulating signals present in the i.f. signals.

The present invention is based on the realisation that the signal equaliser will attempt to overcome all the distortion occurring in the path of the signal from the point when it leaves the transmitter until it enters the equaliser. Hence it is possible to increase the width of the notch by using a low value capacitor and thereby reducing the effect of the ac coupling time constant on the recovery of the receiver from a change in dc offset caused by amplitude or pulsed interfering signals whilst recovering the modulating signal substantially undistorted.

The receiver may have various architectures such as a phasing receiver or a polyphase receiver.

The amount of the frequency offset may be chosen to place any known interfering signals at one edge of, or beyond, the bandwidth of the wanted signals.

In an embodiment of the present invention the means for recovering the wanted i.f. signals comprises polyphase filtering means, which may be implemented as gyrator filtering means or as transconductor integrator filtering means, and which is able to provide a complex output signal in response to a complex input signal and can effectively filter out the image of the wanted signal.

The present invention will now be described, by way of example, with reference to the accompanying draw-

ings, wherein;

Figure 1 is a block schematic diagram of a basic direct conversion ZIF receiver,

Figure 2A shows the signal received at the antenna,

Figure 2B shows the signal at the output of the mixers,

Figure 3 is a block schematic diagram of one embodiment of an integrated receiver made in accordance with the present invention,

Figure 4 illustrates a known symmetrical polyphase filter,

Figure 5 illustrates another known symmetrical polyphase filter fabricated using gyrators,

Figure 6 is a block schematic diagram of another embodiment of an integrated receiver made in accordance with the present invention, and

Figures 7A and 7B are waveform diagrams explaining the operation of the circuit shown in Figure 6, and

Figure 8 is a block schematic diagram of transconductor integrator filters.

In the drawings the same reference numerals have been used to indicate corresponding features.

For convenience of description the present invention will be described with reference to the GSM digital cellular telephone system.

The zero i.f receiver shown in Figure 1 comprises an antenna 10 which is coupled to an rf bandpass filter 12 which selects the band of frequencies of interest. The output from the bandpass filter 12 is split into two paths I, Q, each of which has a mixer 14, 16. First inputs of the mixers 14, 16 are coupled to the output of bandpass filter 12. The second inputs of the mixers 14, 16 are provided by a local oscillator signal from an oscillator 18. The local oscillator signal supplied to the mixer 14 is phase shifted by approximately 90° relative to that applied to the mixer 16 by means of a 90° phase shifter 20. The products of mixing are applied to respective low pass filters 22, 24, the outputs of which are supplied to a demodulator 26 which provides the wanted signal as an output on a terminal 28.

The operation of this type of receiver is well known. The local oscillator frequency corresponds approximately to the nominal carrier frequency of the signal received at the antenna 10 and this causes the input signal to be frequency down converted to substantially ZIF.

As mentioned in the preamble one problem with the basic receiver shown in Figure 1 is that of dc offsets. If ac coupling is provided between the mixers 14, 16 and their respective low pass filters 22, 24, then a notch will be created. As was explained if the ac coupling is done by way of capacitors then the width of the notch can be reduced by using high value capacitors but this has the disadvantage of making the receiver circuit slow to respond and also there is a difficulty in integrating high value capacitors. The alternative of using low value capacitors brings the benefits of making the capacitors integratable and speeding up of the circuit but creates a relatively wide notch.

Another problem of this type of receiver arises if the wanted signal bandwidth is relatively close to an interfering source comprising a strong amplitude modulated signal. This is illustrated in Figure 2A which shows in broken lines the rf bandwidth RFBW of the bandpass filter 12. Within the bandwidth RFBW lies the wanted signal which is a frequency modulated signal, symmetrically disposed about a nominal carrier frequency F_W, upper and lower adjacent channels centred on nominal carrier frequencies F_H and F_L, respectively, and a strong amplitude modulated signal comprising a carrier F_U and sidebands referenced F_{AMP}. Figure 2B shows the result of frequency down conversion in the mixers 14, 16 using a local oscillator frequency at or about F_W, the signal components below F_W are folded about zero frequency so that the higher and lower frequency halves of the wanted signal overlie each other, the higher and lower adjacent channels F_H and F_L are superposed on one another and, as a result of direct detection, the amplitude modulated component F_{AMP} of the unwanted signal lies within the bandwidth of the wanted signal. The unwanted signal F_{AMP} cannot be removed by channel filtering without affecting the wanted signal because it is lying within the bandwidth of the wanted signal.

One method of alleviating this problem is to move the wanted i.f. band of frequencies away from ZIF and to make it higher than that of the directly detected interferer F_{AMP}. If this is done then a high pass filter can be used to separate the wanted signal from the unwanted signal. However a high pass filter is effectively equivalent to using a low value capacitor to provide ac coupling which in turn leads to the creation of a wide notch which would lead to the creation of an unwanted image response which would need to be suppressed.

Two possible methods of providing this image suppression are the use of a phasing or a polyphase receiver.

Figure 3 illustrates a phasing receiver in which the local oscillator signal is selected to provide an intermediate frequency which is higher than, and separate from, the unwanted interferer F_{AMP}. The i.f. has a value, for example half the channel spacing, such that the receiver can be fabricated as an integrated receiver.

The phasing receiver comprises an antenna 10 which is connected to a bandpass filter 12 the output of which is connected to first inputs of frequency down converting mixers 14, 16. A local oscillator 18 having a frequency which is offset from the nominal carrier of the wanted signal (F_W+F_{if}) is supplied directly to the second input of the mixer 16 and by way of a 90° phase shifter 20 to the second input of the mixer 14. High pass filters 23, 25 are coupled to the outputs of the mixers 14, 16, respectively. Phase shifting devices 30, 32 are connected to outputs of the high pass filters 23, 25. The rel-

ative phase shift between the phase shifters 30, 32 is approximately 90° but otherwise the actual phase shifts introduced are arbitrary. The outputs of the phase shifters 30, 32 are applied to respective inputs of a summing (or differencing) stage 34 in order to recover the wanted signal which is applied to bandpass filter 36.

As mentioned, the use of high pass filters 23, 25 creates a relatively large notch NO which as shown in Figure 7B distorts the lower frequency end of the wanted band of frequencies. In order to overcome the distortion introduced by the high pass filters together with any other distortion in the signal channel between the transmitter and the antenna 10, an equaliser 52 is coupled to the output of the stage 34. The equaliser 52 may be any suitable type of equaliser such as a Viterbi equaliser or decision feedback equaliser. The filter coefficients of the equaliser 52 are trained using a signal which is suitable for use as a training signal. In the case of GSM, the signal includes a receiver training sequence.

In order for the phasing receiver to be effective sufficient image suppression will need to be achieved. This requires that the mixers 14, 16 should be identical, the phase shift introduced by the phase shifter 20 and the relative phase shift between the phase shifters 30, 32 should each be 90° and lastly the stage 34 should provide perfect addition or subtraction. Even with integrated circuits this cannot be guaranteed. In reality signals are of a complex mathematical nature but the circuit shown in Figure 3 processes the real and imaginary parts of these signals as if they were two separate real signals. In order to be able to deal with complex signals more effectively it is possible for the filters 23, 25, phase shifters 30, 32 and the summing stage 34 to be replaced by a polyphase filter.

Polyphase filters are known per se and Figure 4 illustrates a known symmetrical polyphase filter which is disclosed for example in Figure 3 of British Patent Specification 1174710. The illustrated polyphase filter comprises a four phase network section and each phase comprises a resistor R connected between an input terminal and an output terminal of a phase of which it is associated. A capacitor C couples an input of each phase to the output of an adjacent leading phase. As shown the input voltages V_1, jV_1, $-V_1$, $-jV_1$ and currents I_1, jI_1, $-I_1$ $-jI_1$ are of a complex nature as are the output voltages V_2, jV_2, $-V_2$, $-jV_2$ and currents I_2, jI_2, $-I_2$, $-jI_2$.

Figure 5 illustrates another known symmetrical polyphase filter 50 fabricated using gyrators. This type of polyphase filter is disclosed in a PhD thesis by J.O. Voorman "The Gyrator as a Monolithic Circuit in Electronic Systems" Catholic University of Nijmegen, The Netherlands, 16th June 1977, Pages 91 to 103. The illustrated polyphase filter comprises third order LC channel filters 40, 42 implemented using gyrators and each of the stages of the filter are crosslinked by gyrators 44, 46 and 48. The filter 40 could be in the I path and the filter 42 in the Q path. The LC filter comprises capacitors C10, C12 and an inductance which is simulated by a capacitance C11 and gyrators G10 and G12. The filter 42 is of identical construction and will not be described.

Figure 6 illustrates an integrated polyphase receiver having the same front end as the receiver shown in Figure 3 and in the interests of brevity it will not be described again. The outputs of the mixers 14, 16 are coupled by respective capacitors 54, 56 to inputs of a polyphase filter 50. Outputs from the polyphase filter 50 are coupled to an equaliser and detector 52 to reduce or eliminate distortion which has occurred and to recover the wanted signals.

In Figure 6 F_{if} is passed by the polyphase filter 50 but $-F_{if}$ is blocked more effectively than would be the case in a phasing receiver. The value of F_{if} is selected to be half the channel spacing. Thus in the case of GSM where the channel spacing is 200kHz, F_{if} is 100kHz.

Figure 7A illustrates diagrammatically the outputs of each of the mixers 14, 16. The directly detected AM interferer F_{AMP} is at or adjacent to the lower frequency end of the band of wanted signals which is generally symmetrical about F_{if}. Also shown are the higher and lower adjacent channels centred on nominal carrier frequencies F_H and F_L for the case of choosing F_{if} as half the channel spacing. S represents the degree of image suppression by the polyphase filter.

Figure 7B illustrates the effect of the ac-coupling (curve AC) using a low value of capacitance which produces a notch NO of sufficient width that it distorts the lower frequency half of the band of wanted signals and substantially eliminates F_{AMP}. The lower the value of the capacitors 54, 56, the wider the notch NO which is created which in turn leads to a greater distortion of the wanted signal band. By coupling the equaliser 52 to the output of the polyphase filter 50 then the effects of the distortion introduced by the ac coupling capacitors 54, 56 can be substantially alleviated because the equaliser 52 endeavours to equalise the received signal in respect of all the sources of distortion and not only that which occurs due to the signal channel between the transmitting and receiving antennas. Thus the output from the equaliser 52 comprises a substantially undistorted interference free signal. In the case of GSM, the signal transmitted by a base station includes a training sequence which can be used to train the equaliser coefficients in response to the multipath effects between the transmitting and receiving antennas together with the distortion introduced by the ac coupling capacitors 54, 56. The equaliser 52 may comprise any suitable equaliser such as a Viterbi or a decision feedback equaliser.

Figure 8 illustrates the polyphase filtering means being implemented as third order transconductor integrator filtering means. The in-phase I and quadrature phase Q sections are substantially identical apart from the polarity of the input signals to some of the transconductors.

For convenience of description the in-phase I section will be described in detail and primed reference numerals will be used to indicate the corresponding

parts in the quadrature-phase Q section. The input signal I_{IN} (Q_{IN}) is applied to a non - inverting input 60 (60') of a transconductor 62 (62'). An inverting input 64 of the transconductor 62 is provided with a signal fedback from an output 66 of an integrator 68. An output 70 of the transconductor 62 together with outputs 72, 76 of transconductors 74, 78, respectively, are summed at a node 80 and the sum signal is applied to an input 82 of the integrator 68. In Figure 8 each of the integrators comprises a op-amp A with a shunt capacitor SC.

The output 66 of the integrator 68 is coupled to non-inverting inputs of transconductors 78' and 84 and to the inverting input 64 of the transconductor 62. The inverting input of the transconductor 78' is connected to ground. The output 66' of the integrator 68' is coupled to the inverting input of the transconductor 64' and 78, and to the non - inverting input of the transconductor 84'. The non - inverting input of the transconductor 78 is connected to ground.

The output of the transconductor 84 is coupled to a summing node 86 to which an output of another transconductor 88 is connected. The summing node 86 is coupled to an integrator 90, the output of which is coupled to an inverting input of the transconductor 74 and to non - inverting inputs of transconductors 88' and 92. The output of the integrator 90' is coupled to the inverting inputs of the transconductors 74' and 88 and to the non - inverting input of the transconductor 92'. The non - inverting inputs of the transconductors 74, 74' are connected to ground as are the non - inverting and inverting inputs of the transconductors 88, 88', respectively.

Outputs of transconductors 92, 94 are coupled to a node 96 which is coupled to the input of an integrator 98. An output of the integrator 98 is coupled to the non - inverting inputs of the transconductors 84 and 92 and to the non - inverting input of a transconductor 94'. An output of the integrator 98' is coupled to the inverting inputs of the transconductors 84', 92' and 94. The non - inverting and inverting inputs of the transconductors 94, 94', respectively, are connected to ground. The outputs I_{OUT}, Q_{OUT} are also derived from the outputs of the integrators 98, 98', respectively.

If desired the transconductor integrator filters may have counterparts in switched capacitor, switched current and related digital implementations.

From reading the present disclosure, other modifications will be apparent to persons skilled in the art. Such modifications may involve other features which are already known in the design, manufacture and use of integrated receivers and component parts thereof and which may be used instead of or in addition to features already described herein. Although claims have been formulated in this application to particular combinations of features, it should be understood that the scope of the disclosure of the present application also includes any novel feature or any novel combination of features disclosed herein either explicitly or implicitly or any generalisation thereof, whether or not it relates to the same invention as presently claimed in any claim and whether or not it mitigates any or all of the same technical problems as does the present invention. The applicants hereby give notice that new claims may be formulated to such features and/or combinations of such features during the prosecution of the present application or of any further application derived therefrom.

Claims

1. A receiver comprising means for frequency down-converting a received signal to produce quadrature related i.f. signals at a frequency offset from d.c, means for blocking dc-offsets in the quadrature related i.f. signals, means for recovering the wanted i.f. signals and means for equalising the wanted i.f. signals and detecting modulating signals present in the i.f. signals.

2. A receiver as claimed in Claim 1, characterised in that the receiver is a phasing receiver.

3. A receiver as claimed in Claim 1, characterised in that the receiver is a polyphase receiver.

4. A receiver as claimed in Claim 3, characterised in that the means for recovering the wanted if signals comprises polyphase filtering means, and in that the dc blocking means comprises ac coupling means coupling the outputs of the frequency down-converting means to the polyphase filtering means.

5. A receiver as claimed in Claim 4, characterised in that the polyphase filtering means comprises gyrator filtering means.

6. A receiver as claimed in Claim 4, characterised in that the polyphase filtering means comprises transconductor integrator filtering means.

7. A receiver as claimed in any one of Claims 1 to 6, characterised in that the equalising means comprises Viterbi equalising means.

8. A receiver as claimed in any one of Claims 1 to 7, wherein a source of local oscillator frequency is coupled to the means for frequency down-converting a received signal, characterised in that said source is tunable to generate a local oscillator frequency having a value to down-convert wanted received signals to an i.f. signal of substantially half the channel separation frequency.

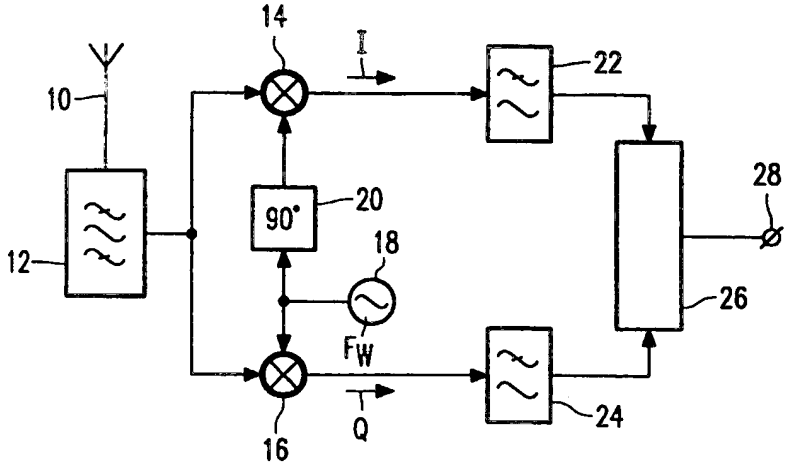


FIG. 1

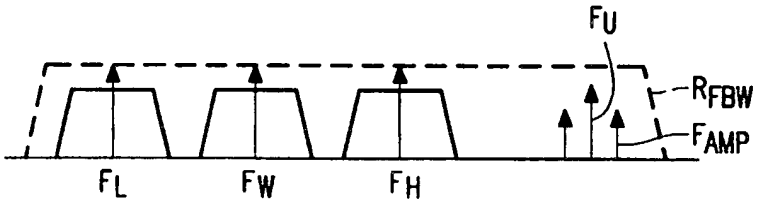


FIG. 2A

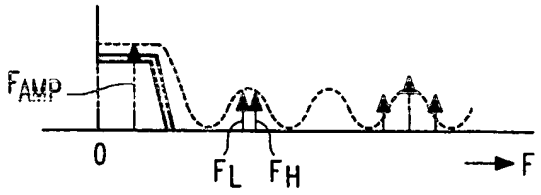


FIG. 2B

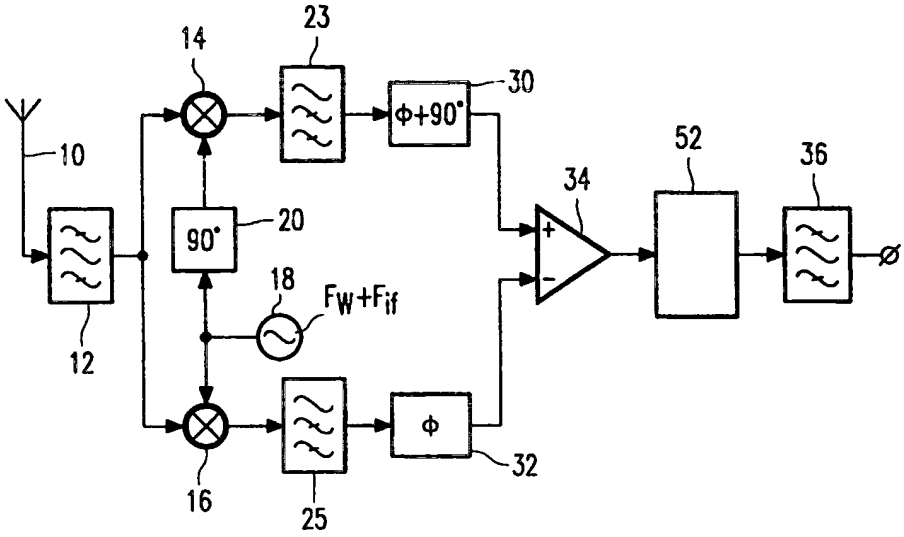
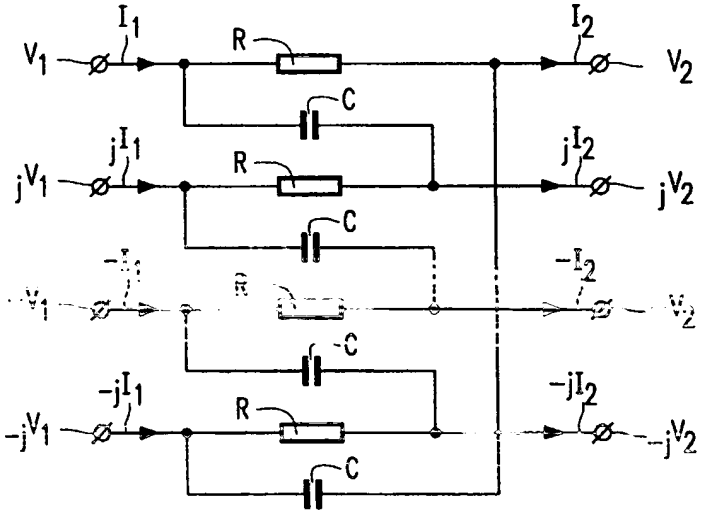

14
23
30
10
φ+90°
52
36
34
90°
20
18
F_W+F_{if}
12
φ
32
16
25

FIG. 3


I_1
R
I_2
V_1
V_2
C
jI_1
jI_2
jV_1
jV_2
$-I_1$
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$-C$
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$-jI_2$
$-jV_1$
$-jV_2$

FIG. 4

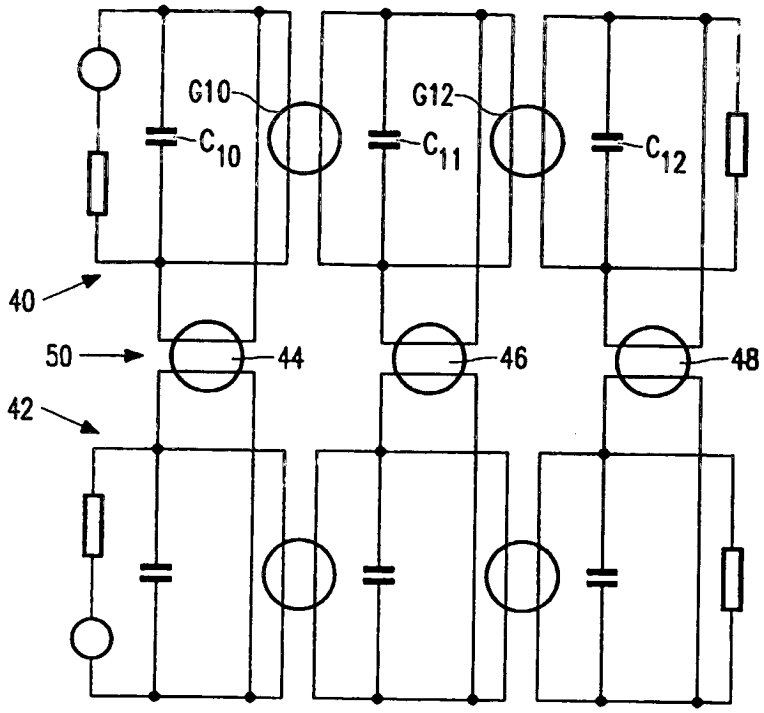
G10
G12
C_{10}
C_{11}
C_{12}
40
50
44
46
48
42

FIG. 5

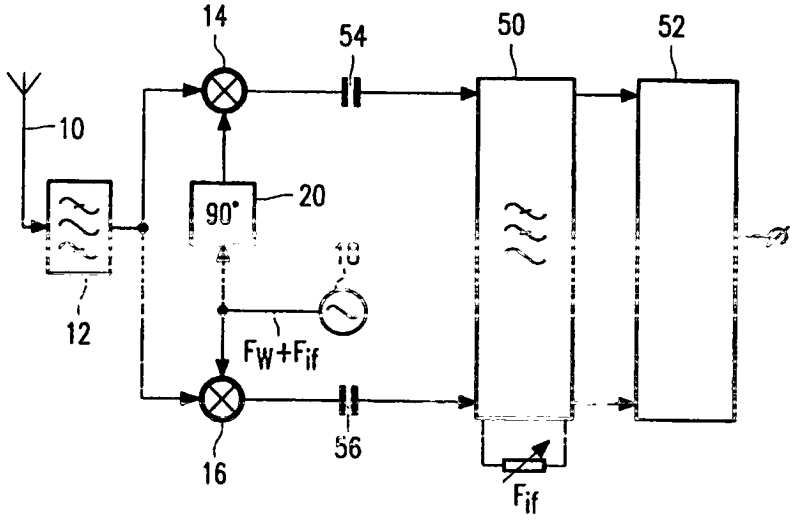
14
54
50
52
10
90°
20
18
12
F_W+F_{if}
16
56
F_{if}

FIG. 6

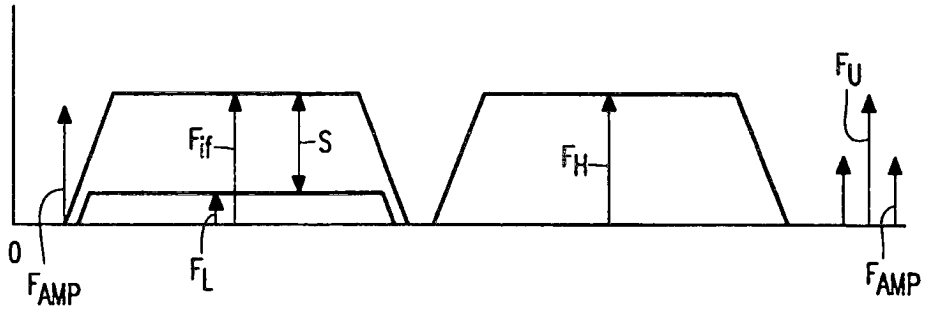

FIG. 7A

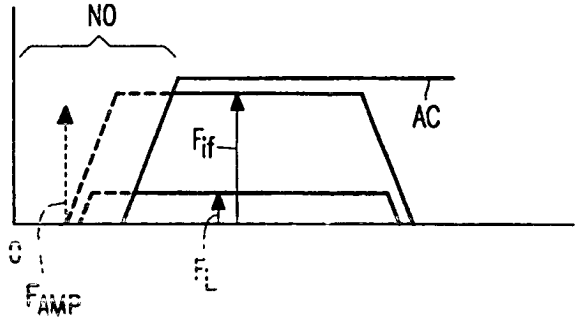

FIG. 7B

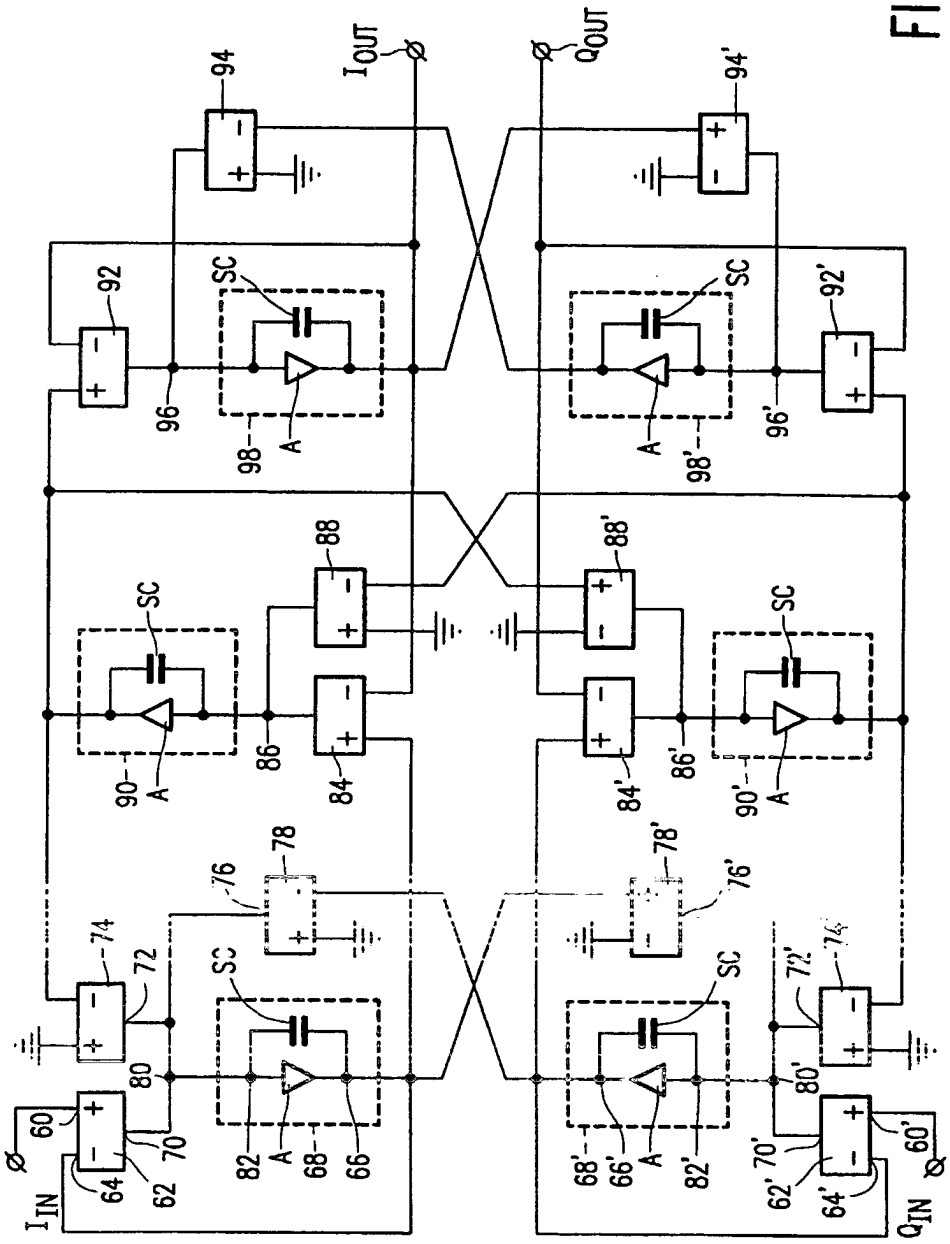

FIG. 8

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 97 20 0613

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	EP 0 595 277 A (HAGENUK GMBH) 4 May 1994 * column 3, line 25 - line 51 *	1,8	H03D3/00
A	ELECTRONICS WORLD AND WIRELESS WORLD, vol. 100, no. 1696, 1 March 1994, pages 202-206, XP000439574 "POLYPHASE DIRECT CONVERSION SSB" * the whole document *	1-4	
A	WO 94 29948 A (RCA THOMSON LICENSING CORP ;ASCHWANDEN FELIX (CH)) 22 December 1994 * abstract; figure 5 *	1	
D,A	US 4 944 025 A (GEHRING MARK R ET AL) 24 July 1990	1	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

H03D

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	9 June 1997	Peeters, M

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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